

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In the application of:

Bert M. VERMEIRE et al.

Serial No.:

Filing Date: November 19, 2003

For: PROGNOSTIC CELL FOR  
PREDICTING FAILURE OF  
INTEGRATED CIRCUITS

Examiner: Unknown

Group Art Unit: Unknown

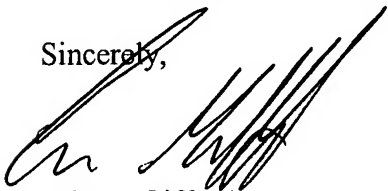
**INFORMATION DISCLOSURE STATEMENT COVER LETTER**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the indicated date. Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This statement should not be construed as a representation that a search has been made, that information cited in the statement is considered to be and/or is material to patentability, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith. It is further understood that the Examiner will consider information that was cited or submitted to the U.S. Patent and Trademark Office in a prior application relied on under 35 U.S.C. §120. 1138 OG 37, 38 (May 19, 1992)."

Sincerely,



Eric A. Gifford  
Registration No. 33,501

11770 E. Calle Del Valle  
Tucson, AZ 85749  
Tel: 520-760-1754  
Fax: 520-844-8644

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Completion if Known**

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)	<b>Applicant Number</b>		
	<b>Filing Date</b>		November 19, 2003
	<b>First Named Inventor</b>		Bert M. VERMEIRE
	<b>Art Unit</b>		Unknown
	<b>Examiner Name</b>		Unknown
<b>Sheet</b>	1	<b>of</b>	2
<b>Attorney Docket Number</b>			300-01-1-001

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	1	V. C. TYREE, "Self stressing test structure cells", Rome Laboratory, Air Force Materiel Command, February 1995, New York.	
	2	T. P. MA et al., "Ionizing Radiation Effects in MOS Devices and Circuits", John Wiley and Sons, 1989.	
	3	G. ANELLI et al., "Radiation tolerant VLSI circuits in standard deep submicron CMOS technologies for the LHC experiments: Practical design aspects," IEEE Trans. Nucl. Sci., vol. 46, pp. 1690-1696, 1999.	
	4	G. S. SHARE, "Effects of Ionizing Radiation on Thin Oxide (20- 1500 Å) MOS Capacitors," J. Appl. Phys., vol. 45, pp. 4894, 1974.	
	5	R. C. LACOE et al., "Total-dose radiation tolerance of a commercial 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 1998.	
	6	R. C. LACOE et al., "Total-dose tolerance of a Chartered Semiconductor 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 1999.	
	7	R. C. LACOE et al., "Application of Hardness-By-Design Methodology to Radiation-Tolerant ASIC Technologies," IEEE Trans. Nucl. Sci., vol. 47, pp. 2334-2341, 2000.	
	8	R. C. LACOE et al., "Total-dose tolerance of the commercial Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 mm CMOS process," presented at Radiation Effects Data Workshop, 2001.	
	9	J. W. R. DAWES et al., "Process technology for radiation-hardened CMOS integrated circuits," IEEE J. Solid State Circuits, vol. SC-11, pp. 459, 1976.	
	10	J.M. BENEDETTO et al., "Mosfet and MOS Capacitor Responses to Ionizing Radiation" IEEE Transactions on Nuclear Science, Vol. NS-31, No. 6, Decemebr 1984.	

<b>Examiner Signature</b>		<b>Date Considered</b>	
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First Named Inventor

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	11	A. MEKKAOUI et al., "30Mrad(SiO <sub>2</sub> ) radiation tolerant pixel front end for the BTEV experiment," Nucl. Instr. and Meth. A, vol. 465, pp. 166-175, 2001.	
	12	J. D. M. FLEETWOOD, "A Reevaluation of Worst-Case Post-irradiation Response for Hardened MOS Transistors," IEEE Trans. Nucl. Sci., vol. NS-34, pp. 1178, 1987.	
	13	K. P. V. DRESSENDORFER, "The Effects of Test Conditions on MOS Radiation Hardness Results," IEEE Trans. Nucl. Sci., vol. NS-28, pp. 4281, 1981.	
	14	M. KIMURA, "Field and Temperature acceleration model for time-dependent dielectric breakdown," IEEE Trans. Electron Devices, vol. 46, pp. 220-229, 1999.	

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